

In The Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-39: CANCELED

40. (Previously Presented) A data processing system comprising:
a data storage medium;
a processing device in communication with the data storage medium; and
a computer system having a system bus, wherein the computer system is configured to communicate with the processing device over the system bus;
wherein the processing device comprises a programmable logic device configured to process the data, as it passes between the data storage medium and the computer system, through a plurality of stages implemented on the programmable logic device as a processing pipeline, each processing stage being dedicated to a different processing operation; and
wherein the processing operations comprise at least two selected from the group consisting of a search operation, a data reduction operation, a data classification operation, an encryption operation, a decryption operation, a compression operation, and a decompression operation.

41. (Original) The system of claim 40 wherein one of the at least two processing operations is a search operation.

42. (Original) The system of claim 41 wherein the data storage medium comprises data stored therein in an encrypted format, and wherein the programmable logic device is further configured to (1) receive a continuous stream of encrypted data from the data storage medium, (2) decrypt the received continuous stream to create a decrypted data stream, and (3) perform a search operation within the decrypted data stream.

43. (Original) The system of claim 42 wherein the search operation is configured to determine whether a pattern match exists between a search key that is representative of data

desired to be retrieved from the data storage medium and a data signal that is representative of the decrypted data stream.

44. (Original) The system of claim 41 wherein the data storage medium comprises data stored therein in an encrypted compressed format, and wherein the programmable logic device is further configured to (1) receive a stream of encrypted compressed data from the data storage medium, (2) decrypt the received stream to create a decrypted compressed data stream, (3) decompress the decrypted compressed data stream to create a decompressed decrypted data stream, and (4) perform a search operation within the decompressed decrypted data stream.

45. (Original) The system of claim 44 wherein the search operation is configured to determine whether a pattern match exists between a search key that is representative of data desired to be retrieved from the data storage medium and a data signal that is representative of the decompressed decrypted data stream.

46. (Original) The system of claim 41 wherein the programmable logic device is an FPGA.

47. (Original) The system of claim 40 wherein one of the at least two processing operations is a compression operation.

48. (Original) The system of claim 40 wherein one of the at least two processing operations is a decompression operation.

49. (Original) The system of claim 40 wherein one of the at least two processing operations is a data reduction operation.

50. (Original) The system of claim 40 wherein one of the at least two processing operations is a data classification operation.

51. (Previously Presented) The system of claim 40 wherein the data storage medium comprises a disk drive system for magnetically storing data, the disk drive system comprising:

a rotatable disk upon which data is magnetically stored in a plurality of discontiguous arcs, wherein each arc possesses a substantially constant curvature, the plurality of discontiguous arcs together defining a generally helical pattern about a central origin;

a device for rotating the disk when data is to be read therefrom;

a read head positioned for reading the data stored on the disk as the disk rotates; and

a positioning system configured to position the read head over the disk such that, as the disk rotates, the read head follows the generally helical pattern of the discontiguous arcs.

52. (Previously Presented) The system of claim 40 wherein a plurality of data files are stored in the data storage medium, each data file being stored as a sequence of segments, each segment having a size that is a power of 2.

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54. (Previously Presented) A hard disk drive accelerator for connection between a hard disk drive and a processor, said accelerator comprising reconfigurable hardware logic arranged such that data read from the hard disk drive streams through the reconfigurable hardware logic prior to being passed on to the processor, wherein the reconfigurable hardware logic is configured to process the data stream through pipeline comprising a plurality of processing stages, each processing stage being configured to perform a data processing operation on the data it receives, and wherein the processing operations performed by the stages of the pipeline are at least two selected from the group consisting of: a search operation, a data reduction operation, a data classification operation, an encryption operation, a decryption operation, a compression operation, and a decompression operation.

55. (Original) The accelerator of claim 54 wherein the reconfigurable hardware logic is implemented on a programmable logic device, wherein the hard disk drive comprises data stored therein in an encrypted format, and wherein the programmable logic device is configured to (1) receive a continuous stream of encrypted data from the hard disk drive, (2) decrypt the

received continuous stream to create a decrypted data stream, and (3) perform a search operation within the decrypted data stream.

56. (Original) The accelerator of claim 55 wherein the search operation is configured to determine whether a pattern match exists between a search key that is representative of data desired to be retrieved from the hard disk drive and a data signal that is representative of the decrypted data stream.

57. (Original) The accelerator of claim 54 wherein the reconfigurable hardware logic is implemented on a programmable logic device, wherein the hard disk drive comprises data stored therein in an encrypted compressed format, and wherein the programmable logic device is configured to (1) receive a stream of encrypted compressed data from the hard disk drive, (2) decrypt the received stream to create a decrypted compressed data stream, (3) decompress the decrypted compressed data stream to create a decompressed decrypted data stream, and (4) perform a search operation within the decompressed decrypted data stream.

58. (Original) The accelerator of claim 57 wherein the search operation is configured to determine whether a pattern match exists between a search key that is representative of data desired to be retrieved from the mass storage medium and a data signal that is representative of the decompressed decrypted data stream.

59. (Original) The accelerator of claim 54 wherein the re-configurable hardware logic is implemented on an FPGA.

60. (Original) The accelerator of claim 54 wherein the processing operation of at least one stage is a search operation.

61. (Original) The accelerator of claim 54 wherein the processing operation of at least one stage is a compression operation.

62. (Original) The accelerator of claim 54 wherein the processing operation of at least one stage is a decompression operation.

63. (Original) The accelerator of claim 54 wherein the processing operation of at least one stage is a data reduction operation.

64. (Original) The accelerator of claim 54 wherein the processing operation of at least one stage is a data classification operation.

Claims 65-97: CANCELED

98. (Previously Presented) The system of claim 40 wherein the programmable logic device is further configured to deactivate a stage of the plurality of stages, whereby the deactivated stage acts as a pass through for the data it receives.

99. (Previously Presented) The system of claim 98 wherein the plurality of stages have an associated order, the order of the stages remaining the same whether any of the stages are deactivated.

100. (Previously Presented) A data processing system comprising:
a data storage medium;
a processing device in communication with the data storage medium; and
a computer system having a system bus, wherein the computer system is configured to communicate with the processing device over the system bus;
wherein the processing device comprises a programmable logic device, the programmable logic device implementing a plurality of data processing stages;
wherein each data processing stage is dedicated to a different data processing operation;
wherein the data processing operations comprise at least two selected from the group consisting of a search operation, a data reduction operation, a data classification operation, an encryption operation, a decryption operation, a compression operation, and a decompression operation;
wherein the processing device is configured to selectively activate and deactivate individual ones of the data processing stages to define a data processing pipeline, wherein a deactivated stage acts as a pass through for the data it receives, and wherein an activated stage

performs the data processing operation to which that stage is dedicated upon the data it receives; and

wherein the programmable logic device is further configured to process data, as it passes between the data storage medium and the computer system, through the defined data processing pipeline.

101. (Previously Presented) The system of claim 100 wherein the programmable logic device comprises an FPGA.

102. (Previously Presented) A hard disk drive accelerator for connection between a hard disk drive and a processor, said accelerator comprising reconfigurable hardware logic arranged such that data read from the hard disk drive streams through the reconfigurable hardware logic prior to being passed on to the processor, wherein the reconfigurable hardware logic is configured to process the data stream through a pipeline comprising a plurality of processing stages, each processing stage being configured to perform a data processing operation on the data it receives, wherein the processing operations performed by the stages of the pipeline are at least two selected from the group consisting of: a search operation, a data reduction operation, a data classification operation, an encryption operation, a decryption operation, a compression operation, and a decompression operation, and wherein the reconfigurable hardware logic is further configured to selectively deactivate a processing stage of the plurality of stages, whereby the deactivated stage acts as a pass through for the data it receives.

103. (Previously Presented) The accelerator of claim 102 wherein the plurality of stages have an associated order within the pipeline, the order of the stages remaining the same whether any of the stages are deactivated.

104. (Previously Presented) The accelerator of claim 103 wherein the reconfigurable hardware logic is further configured to selectively activate a deactivated stage of the pipeline, whereby the activated stage performs the processing operation to which that the stage is dedicated on the data that the activated stage receives.